Fachhochschule Nordwestschweiz
Hochschule für Technik

ime Institut für Mikroelektronik

Mixed Signal-ASICs:

From design to good integrated circuits

Workshop on Affordable Design and Production of Mixed-Signal ASICs for Small and Medium Enterprises (SMEs)

Abstract

When the engineer has finished the design work and the simulation delivers correct results, some people still think that the work is done.
In reality, many other aspects like test methodology, package selection, process tolerances and many more have a strong influence on the product performance and price in volume production.

Considering these aspects right from the beginning can save both, time and money.
In this seminar, experts share their experiences and would also like to listen to and discuss yours.

Dates: *May 17th-18th 2011*
Pricing: *Option 1: Day 1 presentations only - CHF 175.-*
Option 2: Day 1 plus cultural & social events - CHF 250.-
Option 3: Full program (Day 1&2) - CHF 350.-
Venue: *Fachhochschule Nordwestschweiz, Klosterzelgstrasse 2, CH-5210 Windisch*

Design by w@rpstudio.ch

For detailed information and registration please go to www.ms-asics.ch.

Day 1: *Presentations and Workshop*
- *IME www.fhw.ch/ime*
- *Aptasic www.aptasic.ch*
- *D4T Systems www.d4t-systems.com*
- *Serma Technologies www.serma-technologies.com*
- *EDA Solutions www.eda-solutions.com*

Day 2: *Hands-on Training (Tanner EDA www.tannereda.com)*
- *Schematic Entry*
- *Simulation*
- *IC Layout*
- *DRC, LVS*

In collaboration with

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Day 1 - Program description
(morning sessions)

09:00 - 09:30 Open doors and registration [Coffee and croissants]

09:30 - 10:15 Key note speech [H. Schmid]: **"Electrical and Human Feedback"**

"What happens during an R&D project largely depends on the complexity of the project. In this talk, I will explain why increasing project complexity both increases the chance of getting extraordinary results and the chance of getting into extraordinary trouble. Then I will provide an idea as to how to manage a complex project such that the project team can profit from the extraordinary results while being robust against the extraordinary trouble."

10:15 - 11:00 Presentation [R. Grandi]: **"Virtual trip around the IC supply chain"**

"ASIC industrialization is not a simple task as it could appear at first sight: many variables along the way play a crucial role in achieving or not the final goal. The IC supply chain is, yes, forward looking and seems to be quite straightforward but many hidden dependencies and adjustment loops might be needed before being able to master the challenge of a product ramp-up.
The presentation will share some good practices that should be considered from the very beginning of an ASIC project sketch (e.g. test and screening methodologies among others). The earlier you take into account all the industrialization aspects within your project the higher is the chance to have a first time right design."

11:00 - 11:30 Coffee break [Coffee and beverages, networking]

11:30 - 12:15 Presentation [G. Keel]: **"Why ASIC Designs are different"**

"The integration of an electronic system in an ASIC usually saves cost, power and space. This talk explains why ASICs can not copy a discrete circuit with well chosen electronic components. Good ASIC designs must take advantage of the efficient and cheap features and technologies like trimming or switched capacitor circuits to cope with the large absolute tolerances of the the ASIC technologies.
The talk also treats the design flow from the idea to the tested and packaged ASIC."

12:15 - 14:00 Lunch break [Business lunch with sandwiches, networking at Lichthof]

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Day 1 - Program description
(afternoon sessions)

12:15 - 14:00 Lunch break [Business lunch with sandwiches, networking at Lichthof]

14:00 - 14:45 Presentation [P. Kaiser]: **"CAD Methods to Improve Yield"**

"Corner Analysis, Monte Carlo Analysis, Design Centering and Design for long term Reliability are important points to consider when trying to create a robust ASIC. This presentation shows how CAD tools and simulation models can support the designer right from the beginning of a new project."

14:45 - 15:15 Coffee break [Coffee and beverages, networking]

15:15 - 16:00 Presentation [L. v. d.Logt]: **"Model driven test development and simulation"**

"While the IC design flow is fully supported by advanced tools and flows, the test development flow is hardly supported by any type of verification tooling. Getting a flawless industrial test plan executing on the tester platform can be a time consuming process. Although the designer's mixed signal simulations prove to be correct, measurements on tester hardware are required to get all timings and signals correct and may deviate from the simulations. Tedious debugging and lengthy test development cycles are the result of this discrepancy. In this presentation, we show a methodology and tool flow based on test simulation of the entire tester interface. The architecture definition will be explained including the hardware abstraction layers and instrumentation models. It will be demonstrated that test simulation can ease the process of industrializing a test plan."

16:00 - 16:45 Presentation [P. Salome]: **"ESD Challenges for fabless companies"**

"During this presentation, the different ESD targets will be reviewed and discussed. The new requirements as IEC testing at silicon level will be addressed. For getting an ESD robust silicon, these new challenges require to consider ESD at different step of the design flow. The constraints of such an integration will be presented."

17:00 - 18:30 Cultural event [Museum visit, networking]
90min guided visit at Bahnpark Brugg

19:15 - 22:00 Social event [Dinner, networking]
Asian buffet at Restaurant Mekong
Aarauerstr. 50, CH-5200 Brugg

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Day 2 - Program description

09:00 - 09:30 Open doors and registration [Coffee and croissants]

09:30 - 12:00 **Hands-on Tanner EDA tool - Part I**
- Schematic Entry
- Simulation

12:00 - 13:30 Lunch break [Business lunch with sandwiches]

13:30 - 16:00 **Hands-on Tanner EDA tool - Part II**
- IC Layout
- DRC, LVS

For detailed information and registration please go to www.ms-asics.ch.

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Presenters and their biographies
(morning sessions)

Dr. Hanspeter SCHMID was an analog-IC designer with Bernafon AG, Switzerland, until 2005, where he mainly worked on audio low-noise amplifiers, voltage regulators, and a wireless transceiver, and was also responsible for full-system signal integrity. Now he is a Research Fellow at IME/FHNW and a senior lecturer at ETHZ. His main research interests are fast low-power circuits (mainly for sensor electronics), signal integrity in analog signal processing, sigma-delta conversion and mixed-analog-digital signal processing. He also does consulting in industry projects.
In addition to his technical work, he occasionally works as a conflict moderator or facilitator, and he gives communication courses and conflict prevention courses for engineers and for laymen.
Hanspeter Schmid was IEEE CAS Analog Signal Processing Technical Committee Co-Chair from 2008-2010 and still is a committee member; he is an Associate Editor of TCAS-I, a member of the ESSCIRC technical committee, and a Distinguished Lecturer of the IEEE CAS Society.

Roberto GRANDI got his master degree (MSc) in electrical engineering in 1998 at the Swiss federal institute of technology in Zurich (ETHZ).
Since then he has held different functions in the semiconductors industry, with various responsibilities in leading companies (Philips, NXP Semiconductors, DSP Group).
His main focus areas, as a member of innovation committees, have been design for testability (DfT), system on chip (SoC) architectures, system in package (SiP) solutions and the whole industrialization cycle (from concept to mass production) of integrated circuit (IC) projects in CMOS technologies down-to 65nm node.
Since 2009 he is working as head of engineering and program manager at Aptasic SA in Boudry/NE.
In 2010 he got an executive Master of Business Administration (eMBA) in Management and Corporate Finance.

Guido KEEL finished his studies at the ETH Zurich in 1989.
He worked several years in the industry designing analog and digital electronics for medical ultrasound and measurement instrumentation, before he started as an analog-IC designer at Fenner ASIC Design Center.
Since 1996 he works as Research Fellow at the FHNW. His tasks include project acquisition, planning and management as well as design of mixed signal ASICs and systems.
His main interests are in the design and modeling of electronic systems including sensors and actors, low power circuits and signal processing.

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Presenters and their biographies
(afternoon sessions)

Peter KAISER studied at the University of Applied Science in Munich Electronics with the major field Communications Engineering. After his degree as Diplom Ingenieur (FH) he started working with Kontron Electronics as application engineer for electronic CAD systems. In 1990 he started working for Computervision and was attended to key customers in the area simulation of analog and digital circuits. After this, 1993 till 1998, he became an expert in simulation methods for electric and magnetic fields and explored systematical methods to describe and solve unwanted electromagnetic couplings (EMC) at Siemens. To his current field of activity, he came in 1998. He was leading the development for several mixed signal ASIC's in the area of automotive and industrial. He guided the ASIC's starting with the product idea, continuing with the design and ended with the high volume production. In May 2006 he started his own business and has an engineering company for mixed signal ASIC Design. He is representing the Tanner IC Design Software and Aptasic in Germany.

Leon VAN DE LOGT has a MSc. degree in Applied Semiconductor physics from the University of Technology Eindhoven, The Netherlands. He has a long history in digital and analog test engineering for Mixed signal circuits, SoC and SIP designs. Leon worked in the Philips Research labs on test innovation for a variety of consumer and automotive products.
In 2006 he joined NXP semiconductors where he was responsible for the improvement of analogue testing for volume production and he had a leading role in the test innovation program in NXP. Leon is holding more than 10 patents in the field of digital and analog testing.
In 2009 he initiated the foundation of D4T Systems, a start-up with main focus on the automation and simulation of the complete tester-chip interface. Currently, he is director of the company.

Dr. Pascal SALOME received his degree in electrical engineering from the National Institute of Applied Sciences (INSA) of Lyon, France in 1994.
He received his PhD degree in 1998 for his studies on physical phenomena in NMOS transistors submitted to Electrostatic Discharges.
In 1998, he joined the R&D centre of STMicroelectronics to develop ESD protection structures for advanced sub-micron technologies. In 2000, he leaded the ESD/LU group for the IO-cell development.
Since 2005, he has been working as program manager and consultant for SERMA technologies.

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